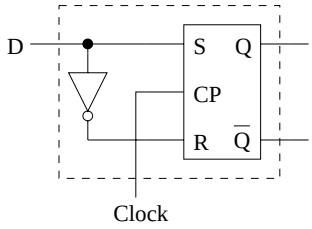
COMP 2003 Computer Organization

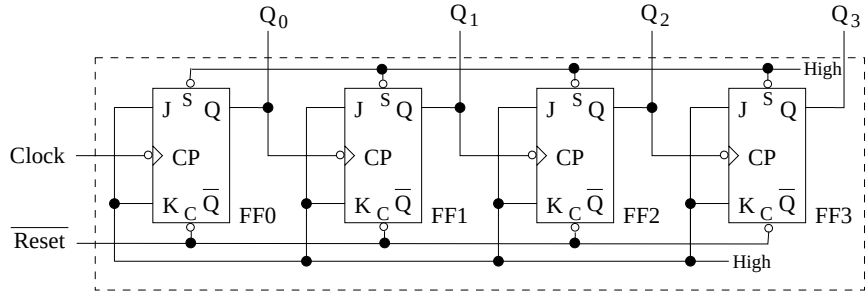
Assignment 2

October 3, 2005

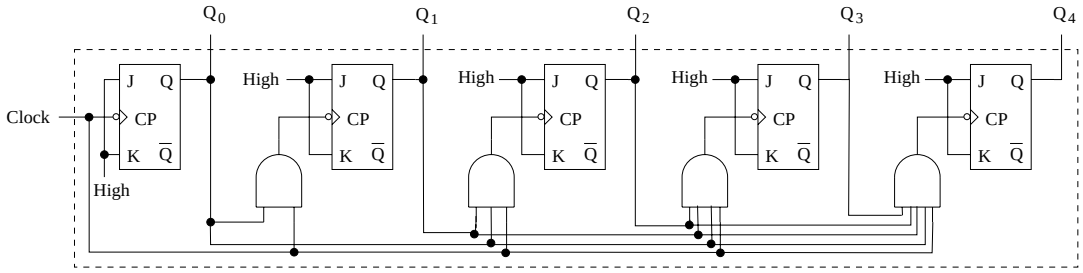
1. The D-latch avoids the SR = 11 input combination by using a single inverter to provide only complementary inputs at S and R inputs of the clocked SR latch as shown below:



2. The circuit is shown below:



3. The circuit is shown below:



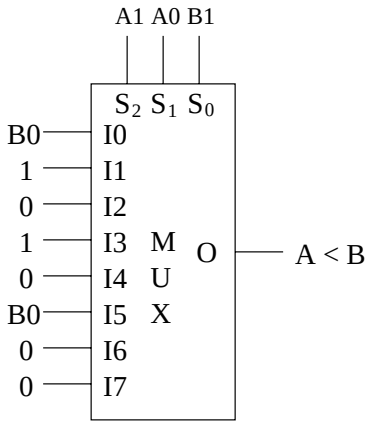
4. The design steps are shown below:

Original truth table

A1	A0	B1	B0	A < B
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Reduced truth table

A1	A0	B1	A < B
0	0	0	B0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	B0
1	1	0	0
1	1	1	0



5. Note that the range of a 2-bit signed number is from -2 to $+1$ as shown below:

A1	A0	value
0	0	0
0	1	1
1	0	-2
1	1	-1

The truth table is shown below:

A1	A0	B1	B0	A<B
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

6. PALs are very similar to PLAs except that there is no programmable OR array. Instead, OR connections are fixed. As a result of this change to the OR array, there is a loss of flexibility that sometimes may cause problems but in practice is not such a big problem. But the advantage of PAL devices is that we can cut down all the OR array fuses that are present in a PLA.

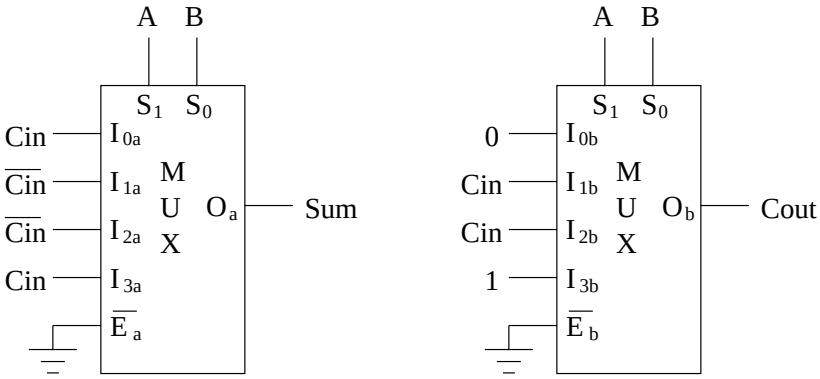
7. The implementation is shown below:

Full adder truth table

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Reduced truth table

A	B	Sum	Cout
0	0	Cin	0
0	1	$\overline{Cin}$	Cin
1	0	$\overline{Cin}$	Cin
1	1	Cin	1



We need an inverter to complement Cin (i.e., to get $\overline{Cin}$).