CARLETON UNIVERSITY
School of Computer Science

COMP 2003A Computer Organization

Fall 2003

Mid-term Examination

Student name: _____

Student number: _____

Notes:

IT IS AN INFRACTION OF THE RULES TO REMOVE THIS EXAMINATION PAPER FROM THE ROOM.

1. This booklet has 9 pages.
2. All questions are to be answered on this booklet. Do not remove any page (even if blank).
3. Use the reverse side of a page if you need more space.

Question	Maximum marks	
Q1	9	_____
Q2	6	_____
Q3	4	_____
Q4	3	_____
Q5	4	_____
Q6	4	_____
Total	**30**	_____

Question 1 [9 points] There is only one correct answer to each question.
Write the letter of the correct answer in the indicated space on the right hand side. (One point per each correct answer.)

1. A processor has 64-bit data bus and 32-bit address bus. All its internal registers are 16 bits wide. Would you say that this processor is a

   a) 16-bit processor b) 32-bit processor c) 64-bit processor
   d) 24-bit processor e) 48-bit processor

   Answer:_____

2. A processor 20-bit address bus. It uses a word-addressable memory where each word is 64 bits wide. What is the memory address space of this processor in bytes?

   a) 1 MB b) 2 MB c) 4 MB
   d) 8 MB e) None of the above

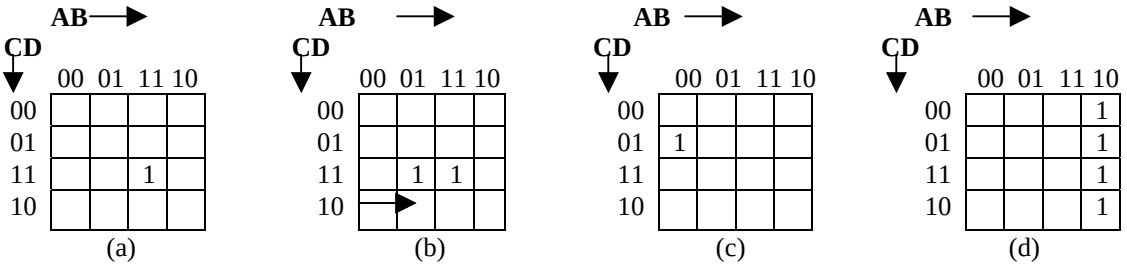
   Answer:_____

3. Suppose that we are storing a variable **`count`** which requires X bytes. When does it make no difference (in how this variable is stored) whether the processor is using the little-endian or big-endian scheme?

   a) X = 1 b) X = 2 c) X = 4
   d) X = 8 e) None of the above

   Answer:_____

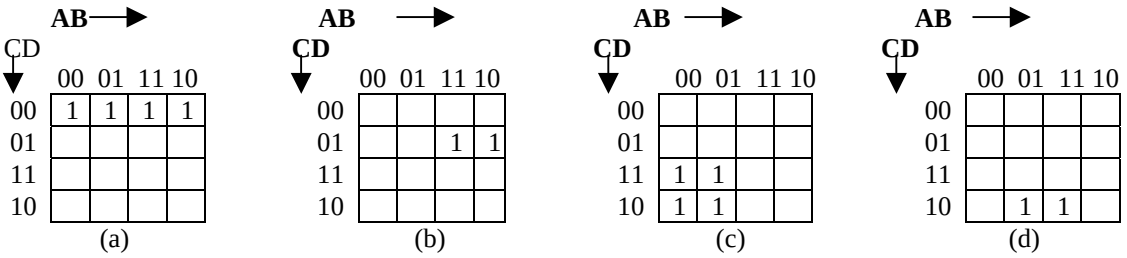
4. Which of the following 4-variable Karnaugh maps below represents the function F(A,B,C,D) = ABCD?



Answer:_____

5. Which of the following 4-variable Karnaugh maps below represents the function

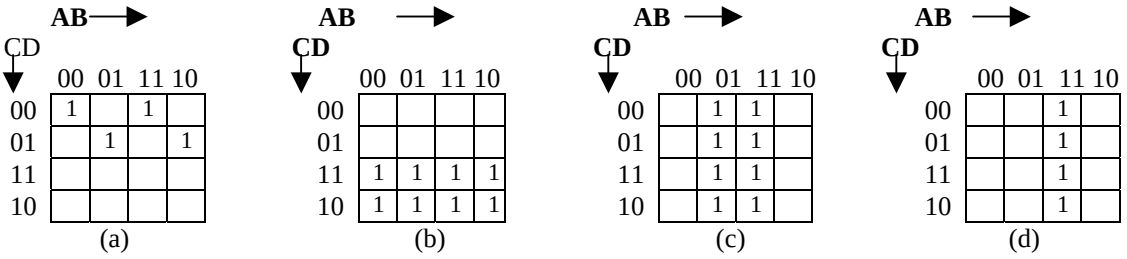
$F(A,B,C,D) = B\overline{CD}$



Answer:_____

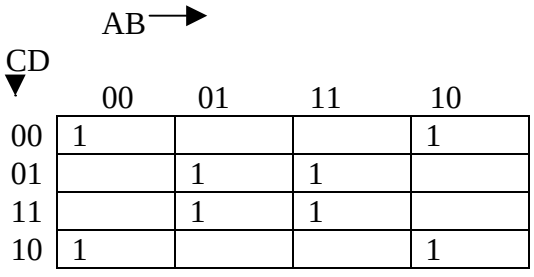
6. Which of the following 4-variable Karnaugh maps below represents the function

F(A,B,C,D) = B



Answer:_____

7. Given the Karnaugh map below, what is the minimized function?



a) $\overline{B}.\overline{D} + B.D$ b) $\overline{A . B} + A.C$ c) $C\,D + A\,B$

d) $\overline{A}\,B + A\,\overline{B}$ e) none of the above

Answer:_____

8. Given the Karnaugh map below, what is the minimized function?

CD \ AB	00	01	11	10
00	1			1
01	1		1	1
11	1		1	1
10	1			1

a) $\overline{A} + BD$ b) $ABC + ACD$ c) $CD + AB$

d) $\overline{B} + AD$ e) $B + ABD$ Answer:_____

9. A set of logic gates is said to be functionally complete if any Boolean function can be implemented by using only the type of gates in the given set. Which of the following, if any, are **NOT** functionally complete?
   a) AND, OR gates
   b) NAND gate
   c) AND, NOT gates
   d) NOR gate
   e) OR, NOT gates

   Answer:_____

Question 2 [6 marks] Short answer questions.

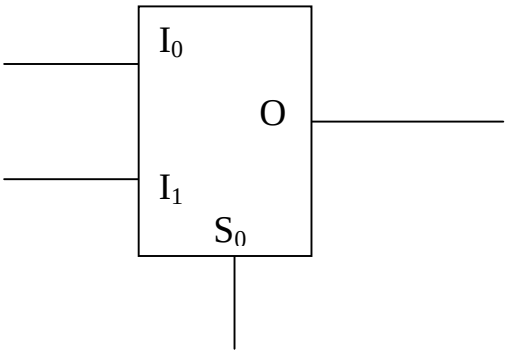
a. Explain why MFLOPS is better than MIPS. (2 marks)

b. Explain why Pentium designers decided to use a 2-address format for its instructions. (2 marks)

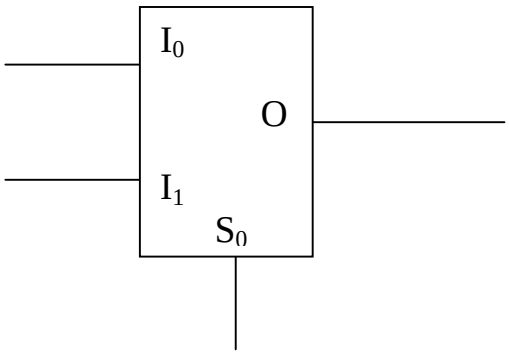
c. Explain the difference between normal branch execution and delayed branch execution. (2 marks)

Question 3 [4 marks] Show that a 2-data input (2 to 1) multiplexer can be used to implement a 2-input AND and a two input OR. Your solution should not use any other gates. Show how each of these gates can be implemented in the space provided below. For your convenience, a 2-data input muliplexer is given. Use this in your implementation.

a) 2-input AND gate implementation Use A and B to label the inputs of the AND gate.



b) 2-input OR gate implementation Use A and B to label the inputs of the OR gate.



Question 4 [3 marks]

Consider two 2-bit numbers A and B. Let a_1 and a_0 represent the two bits in A. a_1 represents the most significant bit and a_0 represents the least significant bit of A. Similarly b_1 and b_0 represent the two bits in B. Give the truth table of a comparator circuit that outputs 1 whenever A >B. Fill in the truth table below.

a_1	a_0	b_1	b_0	F
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Question 5 [4 marks]

Implement the following logical expression

$$AB + BC + AC$$

using three 2-input NAND gates and one 3-input NAND gate. Show how you derived your implementation to get full credit.

Question 6 [4 marks]

Show a 3-bit binary counter using three JK flip-flops. Show all connections to get full credit.