CARLETON UNIVERSITY
School of Computer Science

COMP 2003A Computer Organization

Fall 2003

Mid-term Examination

Student name: _____

Student number: _____

Notes:

IT IS AN INFRACTION OF THE RULES TO REMOVE THIS EXAMINATION PAPER FROM THE ROOM.

1. This booklet has 7 pages.
2. All questions are to be answered on this booklet. Do not remove any page (even if blank).
3. Use the reverse side of a page if you need more space.

Question	Maximum marks	
Q1	4	_____
Q2	6	_____
Q3	6	_____
Q4	9	_____
Q5	5	_____
Total	**30**	_____

Question 1 [4 points] 2 marks each.

a) Given the Karnaugh map below, what is the minimized function?

CD \ AB →	00	01	11	10
00	1			1
01	1			
11	1			
10	1			1

Answer:_____

b) Given the Karnaugh map below, what is the minimized function?

CD \ AB	00	01	11	10
00	1	1		
01	1	1		
11	1	1	1	1
10	1			1

Answer:_____

Question 2 [6 marks] Short answer questions (Use the reverse side if you need more space)

a. Describe the little-endian byte ordering scheme. **(3 marks)**

b. Modern RISC processors use the three-address format. Describe the reasons for this selection. **(3 marks)**

Question 3 [6 marks] Short answer questions (Use the reverse side if you need more space)

a. What is wrong with performance metrics like MIPS? What are the circumstances in which they are useful to compare the performance of processors? **(3 marks)**

b. What is a byte addressable memory? If a processor has a 26-bit address bus and a 16-bit data bus, how much memory (in bytes) can it address? **(3 marks)**

Question 4 [9 marks]
Consider the truth table shown below.

A	B	C	F1
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

a) Write the sum-of-products expression for function **F1**. **(1.5 marks)**

b) Write the sum-of-products expression for function **F1**. **(1.5 marks)**

c) Implement function **F1** using a 3X2 (three inputs and two outputs) PLA with a 8-gate AND array and 2-gate OR array. As in the assignment, you can use the simplified notation to express your design. **(6 marks)**

Question 5 [5 marks] Use the reverse side if you need more space.

a) **(2 marks)** Implement a 3-input NAND gate using three 2-input NAND gates.

b) **(3 marks)** Using the Boolean algebra, show that the following logical expression is equivalent to **AB**.

$$(\mathbf{A} + \mathbf{B})\ \ (\mathbf{A} + \overline{\mathbf{B}})\ \ (\overline{\mathbf{A}} + \mathbf{B})$$