CARLETON UNIVERSITY
School of Computer Science

COMP 2003A Computer Organization

Fall 2003

Mid-term Examination Solution Key

Question 1 [9 marks] 1 mark each

1. A
2. D
3. A
4. A
5. D
6. C
7. A
8. D
9. A

Question 2 [6 marks] (2 marks each)

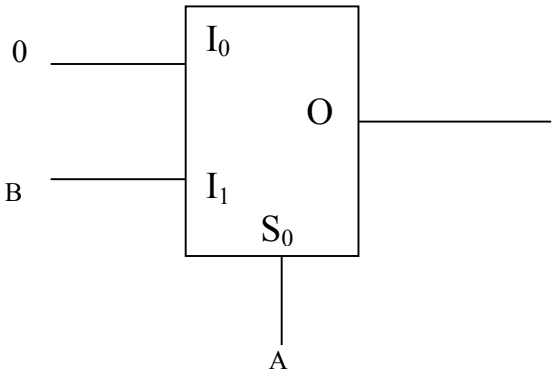
a. MFLOPS stands for millions of floating-point operations per second. This is a far better metric than MIPS as it captures the number of operations in which the user is interested. This measure also takes various system overheads to read operands, store results, and loop testing.

b. One of the reasons is that Pentium provides complex addressing modes. Pentium allows the operands to be in either memory or registers (in contrast to RISC processors, which restrict operands to registers). Instruction length varies depending on the location of the operands. For example, each operand that is memory requires 32 bits to specify its location whereas we need just 3 bits to specify a register. The more addresses there are, the more variability we see in instruction sizes. Another reason is that, in most instructions two addresses are the same as discussed in class.

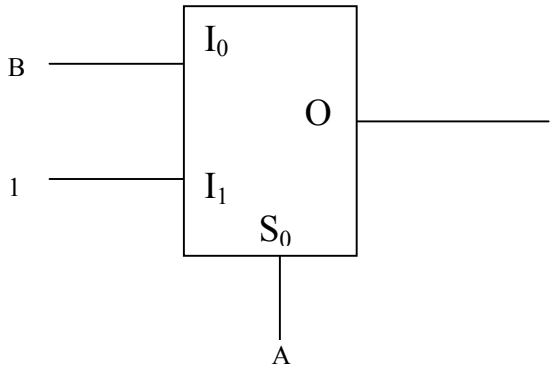
c. In normal branch instructions, the control is transferred to the target instruction immediately after executing the branch instruction. In delayed branch execution, control is transferred to the target after executing the instruction that follows the branch instruction.

Question 3 [4 marks] (2 marks each)

a)



b)



Note: A and B can be interchanged.
No partial marks. Must be correct to get 2 marks. Otherwise, zero marks.

Question 4 [3 marks] (take off 0.2 mark for each wrong answer)

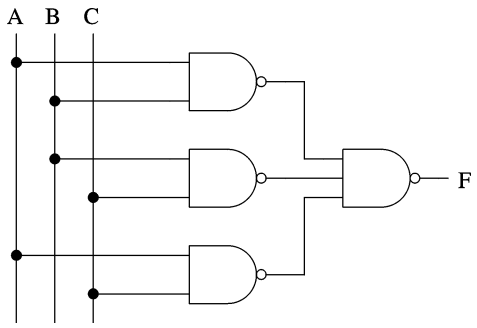
a_1	a_0	b_1	b_0	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Question 5 [4 marks]

Applying de Morgan's law, we derive an expression that is suitable for NAND implementation as shown below: (2 marks for this part)

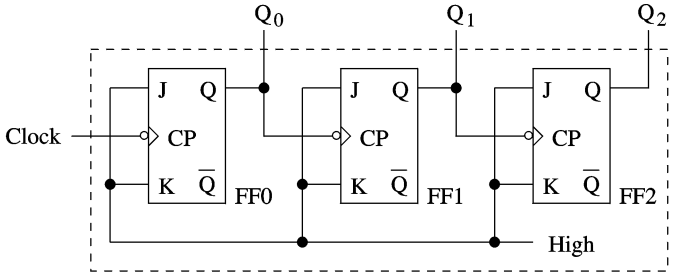
$$\begin{aligned} AB + BC + AC &= \overline{\overline{AB + BC + AC}} \\ &= \overline{\overline{AB} + \overline{BC} \cdot \overline{AC}} \\ &= \overline{\overline{AB} \cdot \overline{BC} \cdot \overline{AC}} \end{aligned}$$

The NAND implementation is shown below: (2 marks for the implementation)



Question 6 [4 marks]

The circuit is shown below:



1 mark for using 3 JK flip-flops

1 mark for showing all three J and K input at 1 (or high)

2 marks for the clock inputs