CARLETON UNIVERSITY
School of Computer Science

COMP 2003 Computer Organization

Fall 2005

Assignment 2

Due date: October 17, 5 PM (MUST be submitted through the Raven system)
Paper assignments will NOT be accepted.

Note: For your convenience, the marking scheme for this assignment is included.

1. How is the D-latch avoiding the input combination S=1 and R=1? (2 marks)

2. Using the 7476 JK flip-flop chips, construct a 4-bit binary counter (just show the logic circuit diagram). This circuit should have a low-active reset input to initialize the counter to 0. (3 marks)

3. Extend the 3-bit synchronous counter shown in Figure 4.15 in the textbook (reproduced in Chapter 4: Slide 21) to implement a 5-bit synchronous counter. (3 marks)

4. Design a 2-bit comparator that outputs 1 when A < B, where A and B are 2-bit unsigned numbers. You design should use only a single 8-input multiplexor. **No additional gates are allowed.** Show all the steps involved in your design, including the truth table and the logic diagram. (6 marks with the following breakdown: truth table --- 2 marks, reduced truth table ---2 marks, logic diagram --- 2 marks)

5. This refers to the last question. In that question, you treated the two input numbers as unsigned. Suppose we treat them as signed numbers (2's complement representation). Give the truth table for this. (3 marks)

6. What is the difference between PLAs and PALs? (2 marks)

7. Implement the full adder, shown in Figure 3.18 (reproduced in Chapter 3: Slide 22) using a 74153 multiplexor chip. You can use an additional inverter in your design. Show all the steps involved in your design, including the truth table and the logic diagram. (6 marks with the following breakdown: truth table --- 2 marks, reduced truth table ---2 marks, logic diagram --- 2 marks)

Total marks = 25